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Research Article

Hardware Implementation Based on FPGA of AES Encryption and Decryption System

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Abstract: It is not hard to predict that AES algorithm will play an important role in information security field for a long time in the future after Rijndael algorithm was announced as advanced encryption standard. Hardware implementation based on FPGA of AES algorithm has the advantages of fast, flexible, short development cycle, etc. Hardware implementation based on FPGA of AES encryption and decryption system was studied in this paper concerning the problem that hardware implementation of AES encryption and decryption algorithm on the basis that the overall structure of AES algorithm, basic transformations, encryption and decryption process were all deeply analyzed. First, implementation scheme and key technology to adopt internal and external mixing pipeline structure were determined, and the overall design flow chart was given. Next, considering different application environment, this design supports three modes of encryption and decryption process of AES algorithm under the condition of data group of 128 bits, key length of 128 bits, 192 bits and 256 bits. Therefore, system optimization design of AES encryption and decryption algorithm was completed on the same piece of FPGA chip; Then, coding work and comprehensive compilation was finished by QUARTUS II development tool, and the simulation results by MODELSIM software was given; Finally, this design realized the balance of resources and speed on the basis of guaranteeing speed and had greater advantages in performance.

Keywords: AES, FPGA, pipeline, encryption algorithm, decryption algorithm

INTRODUCTION

Advanced encryption standard (AES) has undergone the development process from software to hardware implementation since it was taken into effect from May, 2002. Along with network transmission speed is promoted to gigabits orders of magnitude, the requirement of algorithm execution speed is becoming more and more high, password algorithm based on software implementation appears insufficient in performance, therefore it is necessary for people to adopt hardware encryption algorithm, which uses some special optimization techniques (such as pipeline and lookup table, etc.), thus data flow is greatly improved and the generation time of key is reduced[1,2]; In addition, encryption algorithm and corresponding key generation implemented by hardware can be encapsulated into a chip which is not easy to be read or changed by outside attacker, thus will have a higher physical security[3-5]. Therefore, cryptographic algorithms based on hardware implementation have caught widespread attention of the industry. Reconfigurable hardware represented by FPGA has its own inherent characteristics of higher security and speed of hardware and flexibility and maintainability of software, which has become a hot research direction of block cipher algorithm for hardware implementation[6,7]. We introduced FPGA realization method of AES encryption and decryption system in this paper, and the optimization of its speed and resource-intensive processing techniques was discussed.

PRINCIPLE OF AES ENCRYPTION AND DECRYPTION SYSTEM

AES algorithm is a kind of iterated block cipher, which deals with encryption and decryption operations of 128-bit data blocks. As advanced encryption standard, both of data group length and initial key length of Rijndael algorithm are variable. In order to meet the requirements of AES, group length is fixed to 128 bits, key length is respectively represented by 128/192/256 bits.

During the operations of encryption and decryption of AES, first, the inputted data of 128 bytes are first arranged into 4 * 4 byte matrix, then 10 (128 bit key), 12 (192 bit key) or 14 (256 bit key) rounds of transformations are conducted according to different key lengths, the number of round is decided by key length. The implementation of AES encryption algorithm includes key extension process and encryption process[8]. For example, if key length is 128 bits, then encryption process includes an initial round of key addition (AddRoundKey), nine times of round transformations (Round), and the final round of transformation (FinalRound), as shown in Fig. 1.

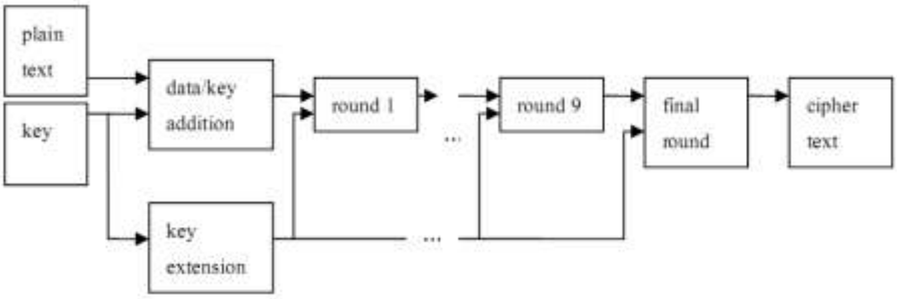

Fig-1: The whole process of encryption (key length is 128 bits)

Every round transformation is composed of four layers, which are listed below. The first layer is byte substitution (SubBytes), meaning that S box whose input is 8 bits, and output is also 8 bits acts on each byte of state matrix; The second and the third layer are respectively ShiftRows, and column transformation (MixColumns), meaning that 4 * 4 state matrix is transformed by line shift and mixed in the column; The fourth layer is key addition (AddRoundKey), meaning that each byte of the key and corresponding byte of state matrix are performed xor operations[9]. The process of each round is shown as Fig. 2.

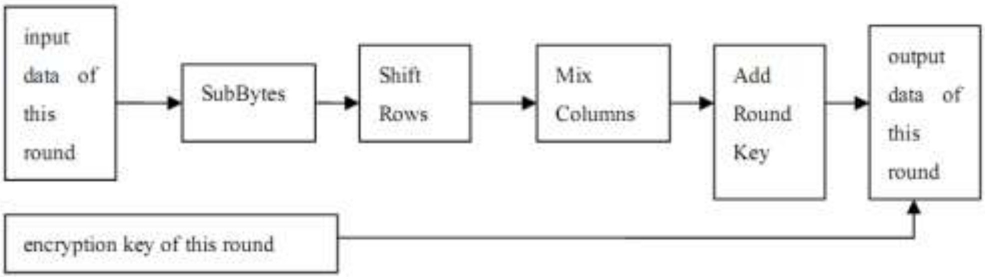

Fig-2: The structure of every round

Similarly, the realization of AES decryption algorithm includes key extension process and ecryption process. Decryption process is similar to encryption process, and is the inverse operation of encryption process. The encryption and decryption process of AES algorithm for data group size of 128 bits and initial key length of 128 bits is shown as Fig. 3.

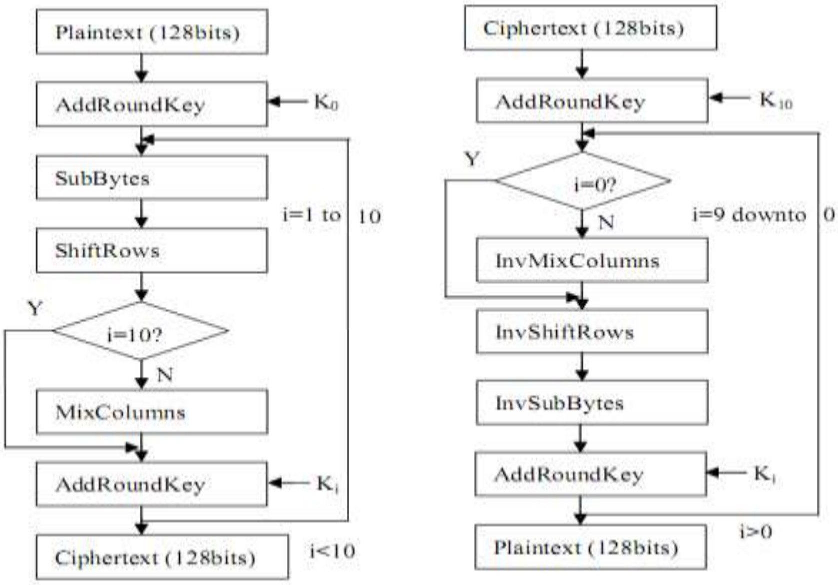

Fig-3:The encryption and decryption process of AES algorithm (128 bits key)

FPGA-BASED IMPLEMENTATION OF AES ENCRYPTION AND DECRYPTION SYSTEM

Hardware implementation of AES encryption and decryption system in this paper is under the condition of satisfying timing requirements, and reducing the whole chip area. Hardware implementation improved the structure of each module within the algorithm and the structure of the whole system. Specifically speaking, it adopts internal and external mixing pipeline, and at the same time, byte substitution, column mixing transformation and key extension operation are respectively optimized to achieve the aim of improving the processing speed of AES encryption and decryption system and realizing the balance between speed and occupied resources[10-12]. The design process of the whole system is shown as Fig.4.

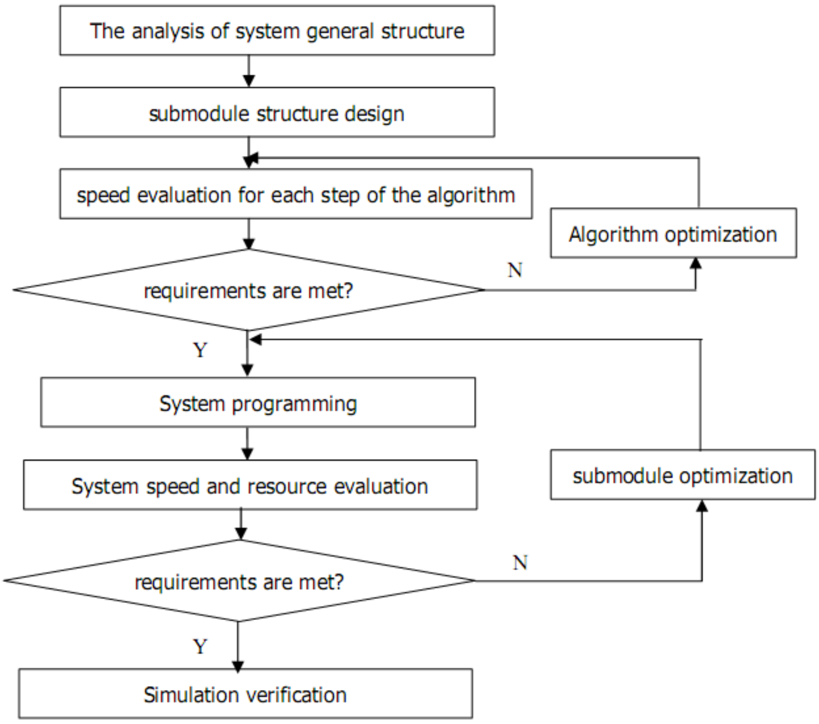
The analysis of system general structure
submodule structure design
speed evaluation for each step of the algorithm
Algorithm optimization
N
requirements are met?
Y
System programming
System speed and resource evaluation
submodule optimization
N
requirements are met?
Y
Simulation verification

Fig-4: System design flow chart

The system is composed of the following modules: data input and output module, encryption and decryption operation module, key extension module, and control unit to control the whole process. Specifically speaking, Control unit generates control signals required for each module; key extension module completes the production and dispatching of keys for each round; encryption and decryption operation module finishes data round transformation[13]. Note that control signals enter from input interface, data and keys come from data bus to conduct data transmission, substitute keys and conduct encryption and decryption operations according to control signals of control modules.

The work pattern and structure of encryption and decryption module

The work pattern of AES algorithm is divided into feedback model and non-feedback. In feedback work pattern, the operations of group encryption and decryption can only be performed in sequence, that is to say, encryption or decryption steps in all the groups must be executed in serial sequence; In the non-feedback work pattern, subsequent group data block operations have nothing to do with previous group data block, therefore all operations can be concurrently performed in theory. In addition, encryption and decryption speed is different under different work patterns. Encryption and decryption speed of AES algorithm refers to the number of bits performed in unit time to complete the encryption or decryption process, or called throughput, also known as a unit for megabits per second (Mbit/s). The structure of encryption and decryption module has a close relationship with its work pattern, whose basic structure can be divided into the following three kinds: external pipeline structure, internal pipeline structure and loop unrolling structure .

The design of encryption and decryption module

In AES encryption and decryption system, in order to improve speed and reduce resource utilization and realize the balance of speed and resource, internal and external mixing pipeline structure based on non-feedback work pattern was adopted. Internal and external mixing pipeline structure of encryption unit is shown as Fig. 5. Similarly, internal and external mixing pipeline structure of decryption unit is shown as Fig. 6.

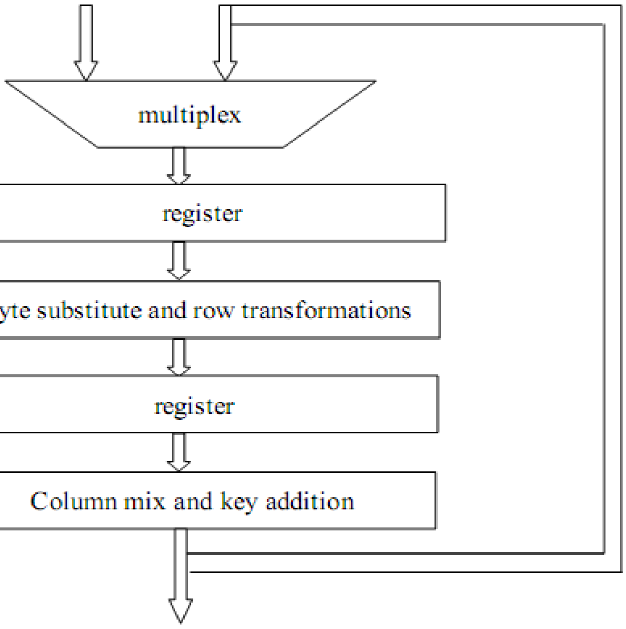
multiplex
register
Byte substitute and row transformations
register
Column mix and key addition

Fig-5: Internal and external mixing pipeline structure of encryption unit

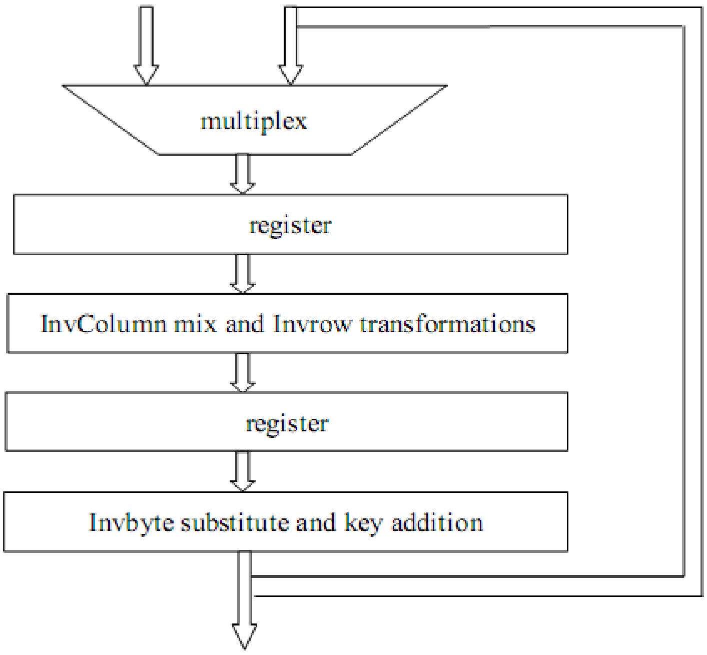
multiplex
register
InvColumn mix and Invrow transformations
register
Invbyte substitute and key addition

Fig-6: Internal and external mixing pipeline structure of decryption unit

SIMULATION RESULTS AND ANALYSIS

First, we performed function simulation with the purpose of verifying the correctness of system logic function. Under the condition of data group of 128 bits, initial key length of 128 bits, system function simulation was performed to verify the correctness of logical function of AES encryption and decryption system. A set of test data used by simulation (using hexadecimal representation) are listed as follows:

Plaintext(128 bits):
3243f6a8885a308d313198a2e0370734;
Key (128bits): 2b7e151628aed2a6abf7158809cf4f3c;
Ciphertext(128bits):3925841d02dc09fbdc118597196a0b32;

Data input and output of encryption part of this system is shown as Fig. 7 and Fig.8.

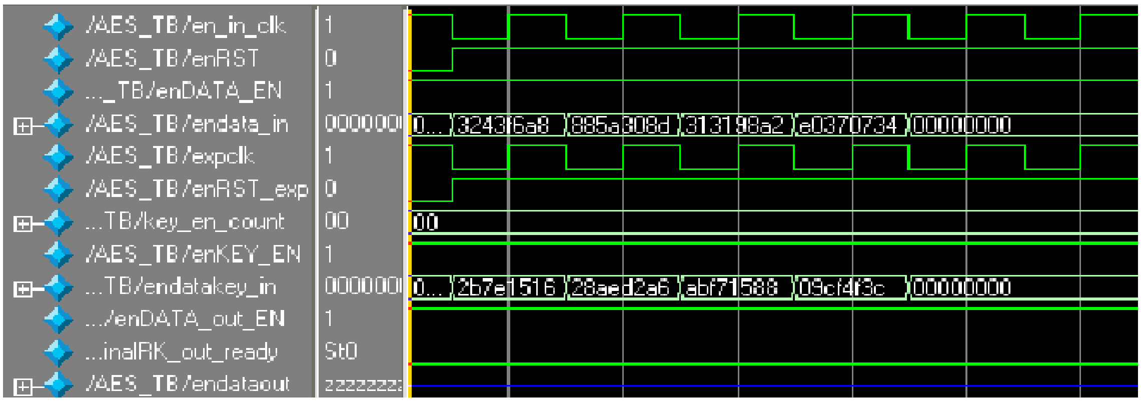

Fig-7: Data input of encryption part of this system

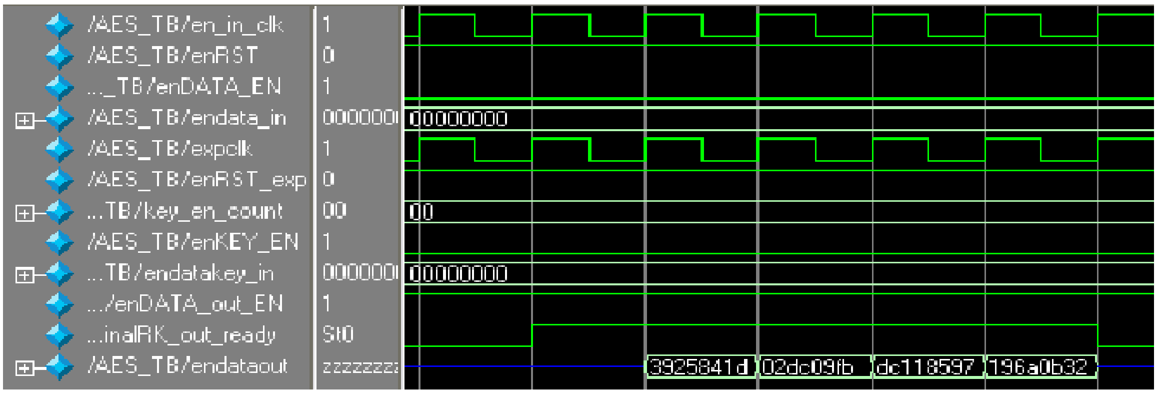

Fig-8: Data output of encryption part of this system

Similarly, data input and output of decryption part of this system is shown as Fig. 9 and Fig.10.

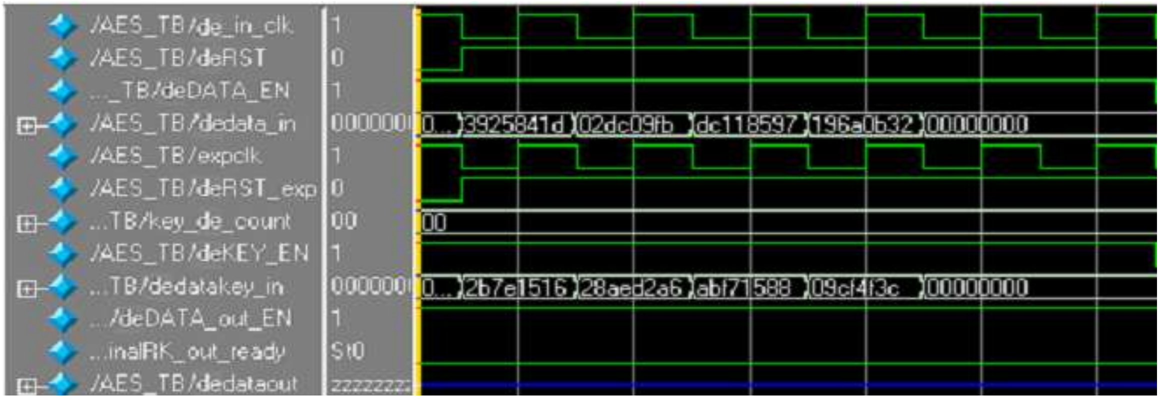

Fig-9: Data input of decryption part of this system

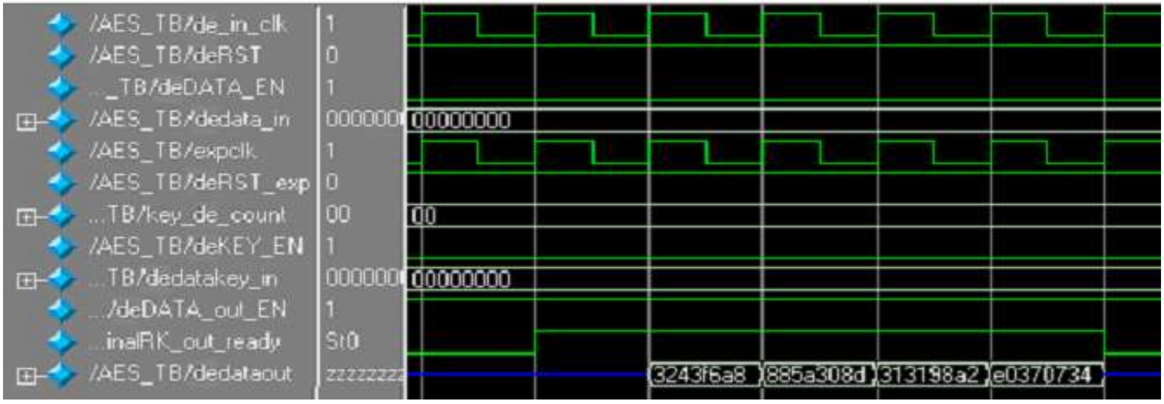

Fig-10: Data output of decryption part of this system

Test results show that this system functions exactly, and correctly implements AES encryption and decryption system to encrypt and decrypt data under the condition of plaintext group of 128 bits, initial key length of 128 bits.

CONCLUSIONS

First, We finished software design code description and comprehensive compilation by QUARTUS software of ALTERA corporation Ⅱ based on the overall structure of AES encryption and decryption system; Next, we performed design simulation by MODELSIM software; Finally, system design and validation results were given. During the design of the whole system, we adopted comprehensive coding style. Open test vector was adopted by function simulation, and the fact that simulation results and test vector data are consistent verified the correctness of system logic functions.

This design does not have the fastest speed, however, its throughput is dominant in general; Furthermore, this design has good speed area ratio; At the same time, the design of the system combines encryption with decryption algorithm, which can be completely executed in parallel. In addition, it achieves the balance of speed and resources under the premise of ensuring encryption and decryption speed.

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REFERENCES

1. Kim H, Hong S, Lim J; A fast and provably secure higher-order masking of AES S-box. Proc. CHES LNCS, Nara, Japan, 2011; 6917:95–107.
2. Carlet C, Goubin L, Prouff E, Quisquater M, Rivain M; Higherorder masking schemes for S-boxes. Proc. FSE LNCS, 2012; 7549: 366–384.
3. Goli JD; Techniques for random masking in hardware. IEEE Trans. Circuits Syst. I, Reg. Papers, 2007; 54(2): 291–300.
4. Canright D, Batina C; A very compact 'perfectly masked' S-box for AES. Proc. ACNS LNCS, 2008; 5037: 446–459.
5. Mangard S, Oswald E, Popp T; Power Analysis Attacks: Revealing the Secrets of Smart Cards. New York: Spinger-Verlag, 2007.
6. Yuan Z, Wang Y, Li J, Li R, Zhao W; FPGA based optimization for masked AES implementation. Proc. IEEE 54th Int. MWSCAS, Seoul, Korea, 2011;1–4.
7. Alam M, Ghosh S, Mohan MJ, Mukhopadhyay D, Chowdhury DR, Gupta IS; Effect of glitches against masked AES S-box implementation and countermeasure. IET Inf. Security, 2009; 3(1):34–44.
8. Trichina E, Korkishko T, Lee KH; Small size, low power, side channel-immune AES coprocessor: Design and synthesis results. Proc. AES LNCS, 2005;3373: 113–127.
9. Mathew SK, Sheikh F, Kounavis M, Gueron S, Agarwal A, Hsu SK, Kaul H et al; 53 Gbps native GF(24)2 composite-field AES-encrypt/decrypt accelerator for content-protection in 45 nm high-performance microprocessors. IEEE J. Solid-State Circuits, 2011; 46(4): 767–776.
10. McLoone M, McCanny JV; Rijndael FPGA implementations utilizing look-up tables. Proc. IEEE Workshop Signal Process. Syst., Antwerp, Belgium, 2001;349–360.
11. Hodjat A, Verbauwhede I; A 21.54 Gbits/s fully pipelined processor on FPGA. Proc. IEEE 12th Annu. Symp. Field-Programm. Custom Comput. Mach., 2004;308–309.
12. Mangard S, Pramstaller N, Oswald E; Successfully attacking masked AES hardware implementations. Proc. CHES LNCS, 2005; 3659:157–171.
13. Oswald E, Mangard S, Pramstaller N, Rijmen V; A side-channel analysis resistant description of the AES S-box. Proc. FSE LNCS, Setubal, Potugal, 2005; 3557:413–423.