Scholars Journal of Engineering and Technology (SJET) **ISSN 2321-435X (Online)**
Sch. J. Eng. Tech., 2016; 4(5):223-227 **ISSN 2347-9523 (Print)**

(An International Publisher for Academic and Scientific Resources)
www.saspublisher.com

Research Article

Trellis-Based QC-LDPC Convolution Codes Enabling Low Power Decoders in Adaptive Technique

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Abstract: Nowadays, in high data rate wireless communication systems, the power consumption of the baseband modems is significantly affected by the channel decoder complexity, especially when codes like LDPC are used. In this paper, we propose a new type of code called Trellis-based Quasi-Cyclic (TQC)-LDPC convolution code, which is a special case of photograph-based LDPC convolution codes. The proposed TQC-LDPC convolution code can be derived from any QC-LDPC block code by introducing trellis-based convolution dependency to the code. The main advantage of the proposed TQC-LDPC convolution code is that it allows reduced decoder complexity and input granularity (which is defined as the minimum number of input information bits the code requires to generate a codeword) while maintaining the same bit error-rate as the underlying QC-LDPC block code ensemble. We also propose two related power-efficient encoding methods to increase the code rate of the derived TQC-LDPC convolution code. The newly derived short constraint length TQC-LDPC convolution codes enable low complexity trellis-based decoders and one such decoder is proposed and described in this paper (namely, QC-Viterbi). The TQC-LDPC convolution codes and the QC-Viterbi decoder are compared to conventional LDPC codes and Belief Propagation (BP) iterative decoders with respect to bit-error-rate (BER), signal-to-noise ratio (SNR), and decoder complexity. We show both numerically and through hardware implementation results that the proposed QC-Viterbi decoder outperforms the BP iterative decoders by at least 1 dB for same complexity and BER. Alternatively, the proposed QC-Viterbi decoder has 3 times lower complexity than the BP iterative decoder for the same SNR and BER. This low decoding complexity, low BER, and fine granularity makes it feasible for the proposed TQC-LDPC convolution codes and associated trellis-based decoders to be efficiently implemented in high data rate, next generation mobile systems.
Keywords: TQC-LDPC, convolution codes, Trellis-Based decoders.

INTRODUCTION

To achieve lower complexity decoder, low BER and fine granularity makes its feasible for the proposed TQC-LDPC convolution codes. Convolution codes are used extensively in numerous applications in order to achieve reliable data transfer, including digital video, radio, mobile communication, and satellite communication [1, 2]. The constructions were the most efficient, coming closest to the Shannon limit. The TQC-LDPC convolution codes in encoder and the qc-viterbi decoder are taken for transmit and to receive the data. The proposed method is by introducing the adaptive viterbi algorithm to decreasing the level in TQC-LDPC convolution code and to increase the fine granularity of the bit and to decrease the power consumption by increasing the speed level.

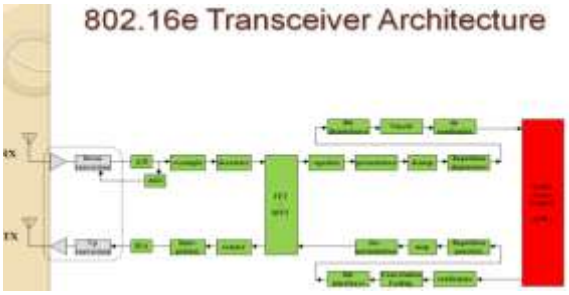

Fig-1: Transceiver Architecture

EXISTING APPROACH

The LDPC codes [3, 10] that are currently implemented in commercial standards are block codes which operate on non-overlapping blocks of bits independently. The block size affects the bit error rate as well as the processing latency. The current LDPC

convolution codes still require high iteration BP-based decoding (i.e., >100 iterations) to achieve low BER which results in large latency, high complexity, and high power consumption.

The new TQC-LDPC convolution code is derived from a given (QC)-LDPC block code by inheriting the LDPC block code parameters that determine the performance of the code. The proposed TQC-LDPC convolution codes offer eight times finer input bit granularity and lower structural latency.

Issues In Existing Technique

- Trellis-based decoding architecture allows us to achieve 8 times finer input bit granularity with significant decoder complexity reduction over conventional LDPC block [16] and convolution codes with iterative BP decoders, while retaining same BER performance and data rate.
- High BER.
- Decoder complexity.
- More power consumption.
- High latency, these are some of the drawbacks in Trellis based Quasi Cyclic Low density Parity Check Convolutional Codes[4, 17].

PROPOSED APPROACH

The analysis and implementation of a reduced-complexity decode approach; the adaptive Viterbi algorithm (AVA).This design is implemented in reconfigurable hardware to take full advantage of algorithm parallelism and specialization. Run-time dynamic reconfiguration is used in response to changing channel noise conditions to achieve improved decoder performance.

Implementation parameters for the decoder have been determined through simulation and the decoder has been implemented on a Xilinx XC4036-based PCI board. An overall decode performance improvement of 7.5X for AVA has been achieved

The new TQC-LDPC convolution code is derived from a given (QC)-LDPC block code [5] by inheriting the LDPC block code parameters that determine the performance of the code. The proposed TQC-LDPC convolution codes offer eight times finer input bit granularity and lower structural latency.

The structure of the new code is designed and proposed a low complexity, non-iterative trellis-based QC-Viterbi decoder. In contrast to iterative BP decoding methods[6, 7] and MAP decoding methods, we believe this is the first non-iterative decoder for LDPC codes that can be applied to low power high data rate systems.

Introduction to LDPC codes

These codes were invented by Gallager in his Ph.D. dissertation at M.I.T. in 1960.They were ignored for many years since they were thought to be impractical. But with present day technology they are very practical. Their performance has some implementation advantages such as Low decoding complexity, Low BER, High data rate [7, 8].

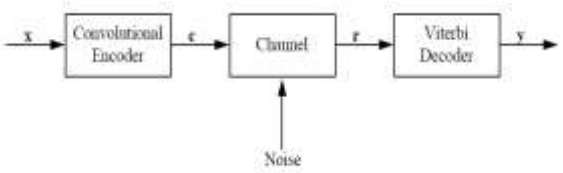

Fig-2: Convolution code system

Fig.2 shows the encoder and decoder structures for convolution codes. The encoder will be represented in many different ways and the main decoding strategy for LDPC convolution codes is based on the Viterbi Algorithm.

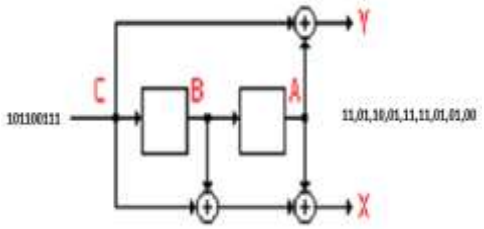

Fig-3: Convolution Encoder; X=A xor B xor C and Y=A xor C

Viterbi decoding error correction

With the aid of the trellis diagram, a received message can be related back to the original bit stream even if the received data contains errors[9, 14]. Assume the circuit starts at 00, and the following short symbol stream is received. Note that the original data bits were 11101100. There are errors in two adjacent bits spanning two symbols, as shown highlighted below the fact is not yet known to the decoder.

11 01 11 11 00 01 01 11

The problem is clear if the symbols are simply accepted as received, as shown below. While the original symbols defined a continuous path through the trellis, the presence of errors means that now there is no obvious continuous path through the trellis. The message bits that the path found will exactly match the original despite the errors which have occurred.

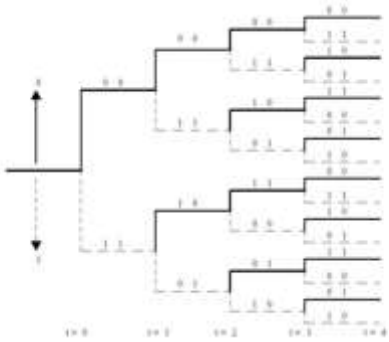

Fig-4: Trellis Diagram

Adaptive viterbi decoder

The AVA only keeps a number of the most likely state instead of the whole of 2k-1 state, where is constraint length of convolution encoder. The rest of the other states are all discarded. The selection is based on the likelihood or metric value of the path, which for hard decision is the hamming distance and a soft decision decoder is Euclidean distance. Truncation length (τ0) controls the average number of path stored per trellis at each stage and the frequency with which trace back length through the trellis is performed. The reason energy consumption can be significantly reduced for adaptive by reducing truncation length is mainly because these parameters greatly affect the number of times path memory is accessed. Actually, the number of time nearly all calculations are performed per trellis stage is proportional to average number of surviving path per stage, which is controlled by truncation length. Fig.5 shows the error decoding technique[11] using viterbi method with adaptive viterbi decoding technique.

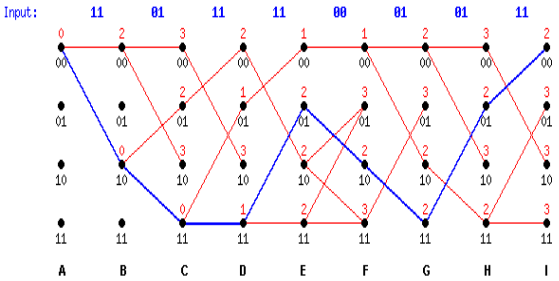

Fig-5: Error Decoding Technique

Adaptive viterbi algorithm

By setting a threshold value v=25, the maximum and minimum distance is calculated between the bit transaction. Take only the level having minimum bit transaction, thus reducing the number of stages [12, 13]. The last output is considered as least distance taken as an original output.

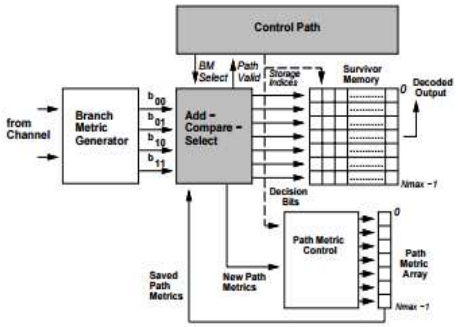

Fig-6: Adaptive Viterbi Decoder

RESULTS AND COMPARISION

Simulation Result of Convolution Encoder

The *clk, rst* are the input to the shift register in the convolution encoder. Shift_reg1 is the 2 bit shit register with i_p as the input of convolution encoder. A data input has passed through the encoder circuit to yield a series of two bit symbols representing each input data as the encoder output en_op1.n1 counts the number of bit encoded.

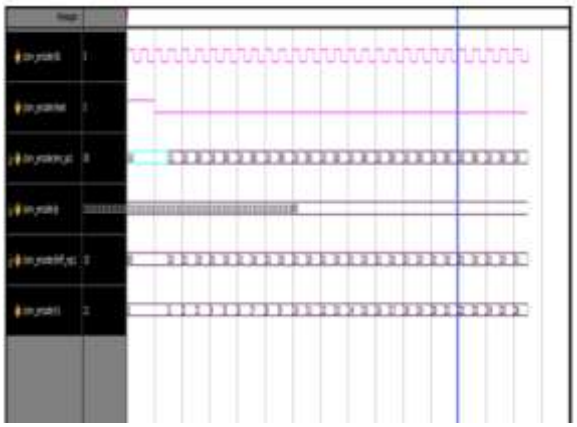

Fig-7: Simulation result of convolution Encoder

Simulation result of viterbi decoder

The *clk* and *en* are the input to the QC-LDPC decoder with i_p as the 2 bit decoder input. The variable *p* is the signal used to store the values of each node in the trellis tree while decoding the data. Count used to calculate the total time needed for decoding while n and r represents the total decoded bit and stages respectively. D is the final decoded output.

Fig-8: Simulation result of viterbi decoder

Simulation result of convolution encoder and viterbi decoder

The *clk*, *rst*, *en* are the input to combined architecture with *ip* as the 1 bit encoder input. A data input has passed through the encoder circuit to yield a series of two bit symbols representing each input data as the encoder output *en_op1* which is given as the input to the decoder. The signal *count* is used to calculate the total time needed for decoding while n and *r* represents the total decoded bit and stages respectively. *OP* is the final decoded output.

Fig-9: Simulation result of convolution encoder and viterbi decoder

The power consumed by belief propagation and QCLDPC and adaptive viterbi decoder are 162mW and 114mW and 112mW respectively. Area occupied by belief propagation and QCLDPC are 565 and 176 and 92 gate count respectively. The delay comparison of belief propagation and QCLDPC [15] are 6.237 ns and 5.422 ns and 4.817ns. The 70% of power consumption is increased comparing to the previous architecture.

Applications

- Wireless Gigabit Alliance
- Wi-Fi
- Wireless personal area networks
- Space research work

Table 1: Power, area and delay comparison of three architectures

Parameters / Types	Delay(ns)	Power(mW)	Area(Gate count)
Belief Propagation	6.237	162	565
QC-Viterbi decoder	5.422	114	176
Adaptive QC-Viterbi decoder	4.817	112	92

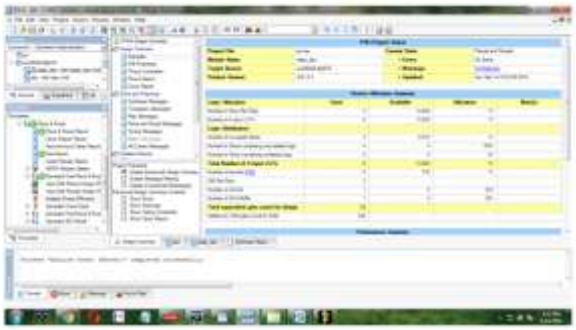

Fig-10: Area report of Adaptive Architechture

Fig-11: Power report of Adaptive Architechture

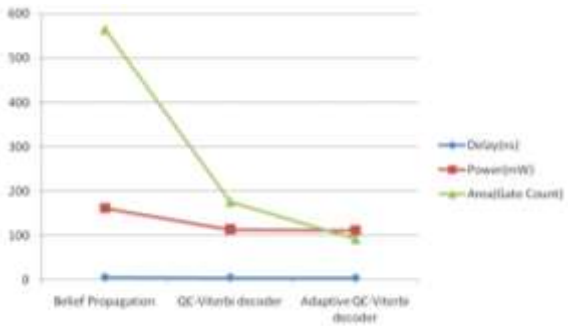

Fig-12: Comparision chart of power, area and delay of three architectures

CONCLUSION

In this paper, a new TQC-LDPC convolution code is introduced. The proposed code coupled with trellis-based decoding architecture allows us to achieve 8

times finer input bit granularity with significant decoder complexity reduction over conventional LDPC block and convolution codes with iterative BP decoders, while retaining same BER performance and data rate. The proposed TQC-LDPC convolution code can be derived from any QC-LDPC block code by introducing trellis-based convolution dependency to the code. The main advantage of the proposed TQC-LDPC convolution code is that it allows reduced decoder complexity and input granularity (which is defined as the minimum number of input information bits the code requires to generate a codeword) while maintaining the same bit error-rate as the underlying QC-LDPC block code ensemble.

REFERENCES

1. Pisek E, Rajan D, Cleveland JR; Trellis-Based QC-LDPC Convolutional Codes Enabling Low Power Decoders. Communications, IEEE Transactions on, 2015; 63(6):1939-51.
2. Feltstrom J, Sh. Zigangirov K; Time-varying periodic convolutional codes with low-density parity-check matrix. IEEE Trans. Inform. Theory, 1999; 45: 2181-2191.
3. Pusane AE, Feltstrom AJ, Sridharan A, Lentmaier M, Zigangirov K, Costello DJ; Implementation aspects of LDPC convolutional codes. Communications, IEEE Transactions on, 2008; 56(7):1060-9.
4. MacKay JDC, Neal RM; Near Shannon limit performance of low density parity check codes. Electron, Lett., 1996; 32:1645-1646.
5. Pisek E, Rajan D, Cleveland JR; Trellis-Based QC-LDPC Convolutional Codes Enabling Low Power Decoders. Communications, IEEE Transactions on, 2015; 63(6):1939-51.
6. He J, Liu H, Wang Z, Huang X, Zhang K; High-speed low-power Viterbi decoder design for TCM decoders. Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, 2012; 20(4):755-9.
7. Wiberg N; Codes and decoding on general graphs. Ph.D. thesis, Linkoping University, Sweden, 1996.
8. Gallager RG; Low-density parity-check codes. IRE Trans. Inform.Theory, 1962; 8: 21-28.
9. Tanner RM; Error-correcting coding system. U.S. Patent # 4, 1981; 295: 218.
10. Tanner RM, Sridhara D, Sridharan A, Fuja TE, Costello Jr DJ; LDPC block and convolutional codes based on circulant matrices. Information Theory, IEEE Transactions on, 2004; 50(12):2966-84.
11. Bates S, Block G; A memory based architecture for low-density parity-check convolutional decoders. in Proc. IEEE International Symposium on Circuits and Systems, Kobe, Japan, May 2005.
12. Chung SY, Forney GD, Richardson TJ, Urbanke RL; On the design of low-density parity-check codes within 0.0045 db of the Shannon limit. IEEE Commun. Lett., 2001; 5:58-60.
13. Chung SY, Richardson TJ, Urbanke RL; Analysis of sumproduct decoding of low-density parity-check codes using a Gaussian approximation. IEEE Trans. Inform. Theory, 2001; 47: 657-670.
14. Richardson TJ, Urbanke RL; The capacity of low-density parity check codes under message-passing decoding. IEEE Trans. Inform. Theory, 2001; 47: 599-618.
15. Richardson TJ, Shokrollahi MA, Urbanke RL; Design of capacity-approaching irregular low-density parity-check codes. IEEE Trans. Inform. Theory, 2001; 47: 619-637.
16. Hehn T, Huber JB; LDPC Codes and Convolutional Codes with Equal Structural Delay: A Comparison. IEEE Transactions On Communications, 2009; 57(6):1683-1692.
17. Kou Y, Lin S, Fossorier M; Low-density parity-check codes based on finite geometries: a rediscovery and more. IEEE Trans. Inform. Theory, 2001; 47:2711-2736.