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Research Article

High Speed Low Power Radix-4 Modified Booth Novel Carry Select Adder Based Multiplier and Multiply Accumulate (MAC) Unit

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Abstract: High speed Low power multiply and accumulate design is the key component of the high performance filter application design. The developed design aims primarily at the improvement in speed of the multiplication and reduction in power dissipation. In this developed design main goal was to find the better solution to the multiply and accumulate (MAC) unit used in filtering units of digital signal processing, image processing etc. The multiply and accumulate unit is developed with radix-4 modified booth multiplier whose partial products are added by the developed novel carry select adder. Most of the filtering applications demand increased speed and reduction in power consumption as the main criteria in their design where developed design supports both the requirements of it.
Keywords: MAC unit, Carry Look Ahead, Modified carry select adder, modified booth multiplier.

INTRODUCTION

Multipliers play very important role in designing the high end applications like microprocessors, controllers, digital signal processing filters, image processing filters etc. where speed of the multiplication and power dissipation are the two crucial factors which has direct impact on the performance of the system. Therefore improving the speed and reducing the power dissipation in VLSI circuits is the main challenge faced by the designers. Since speed, power dissipation and area are the interdependent factors in the VLSI design, optimizing speed indirectly affects the area of the system due to additional circuitries added and additional system's power consumption also adds to the overall system power consumption [1].

Multipliers are one of the important arithmetic unit of the different audio and video processing systems. In most of the digital signal processing systems the multiply and accumulate (MAC) unit is the fundamental unit used for series multiplications of the signal values. In image processing systems the multiply and accumulate (MAC) unit are used for image enhancement, particularly for smoothing the image where image pixels needs to be multiplied along with the neighboring pixels to generate the center pixel of the image window [4].

MODIFIED RADIX-4 BOOTH MULTIPLIER

Modified radix-4 booth's algorithm is twice as fast as the normal booth's algorithm. The radix-4 booth's algorithm reduces the partial products to half of the partial products produced in the normal booth's algorithm. In normal radix-2 booth multiplication, if two 'n' bit numbers to be multiplied, produces 'n' partial products and 'n-1' additions to be performed to produce the product. But modified radix-4 booth algorithm produces only 'n/2' partial products and '(n/2)-1' additions. Hence fast multiplication is made possible. Partial products are obtained on the basis of radix-4 booth encoding table shown in Table 1.

The Multiplier is encoded and with respect to the encoded bits and its operation in the table.1 multiplicand is operated to produce partial products repeatedly.

The addition of the partial products is the main aspect which restricts the speed of the multiplication. In addition of the partial products addition of the bits with carry „0' simply increases one addition more, which can be skipped with the help of the modified carry select adder. Here carry is generated with the help of the carry look ahead logic and the generated carry is used as select input to the multiplexer. The multiplexer

selects the appropriate adder, depending upon the carry produced zero or one. The developed multiplier is shown in Fig.1 [3].

Table 1: Radix-4 Modified Booth Encoding Table

Ai+1	Ai	Ai-1	Operation on Multiplicand (B)
0	0	0	Add zero
0	0	1	Add multiplicand (B)
0	1	0	Add multiplicand (B)
0	1	1	Add 2*multiplicand (2B)
1	0	0	Subtract 2*multiplicand (-2B)
1	0	1	Subtract multiplicand (-B)
1	1	0	Subtract multiplicand (-B)
1	1	1	Subtract zero

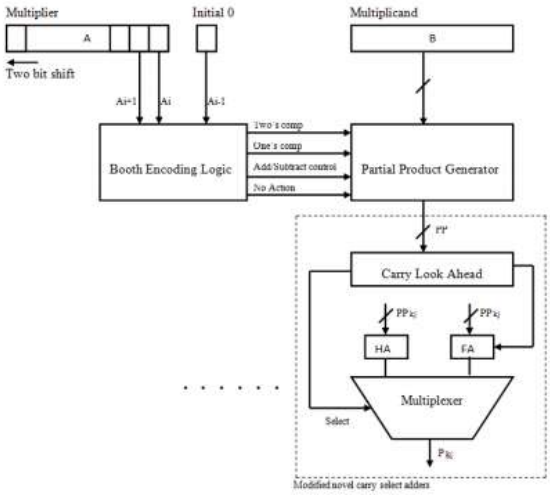

Fig-1: Architecture of the developed multiplier

MULTIPLY AND ACCUMULATE UNIT

The multiply and accumulate unit is one of the frequently used system in digital signal processing filters in which series of successive multiplications are performed. Multiplier combined with add or subtract unit and additional register called accumulator forms the multiply and accumulate (MAC) unit. The MAC unit is shown in Fig 2 [2].

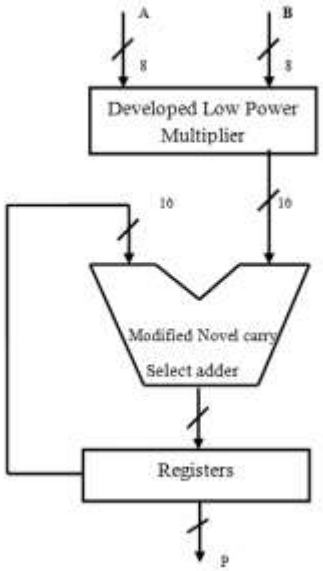

Fig-2: Architecture of the low power MAC unit

In the proposed design multiply and accumulate unit makes use of developed modified novel carry select adder to handle additions with carry bit zero efficiently.

ANALYSIS

The proposed design of high speed was successfully designed and simulated in Xilinx 14.3 ISE design suite for the functional correctness. The operating frequency of the multiplier is high compared to radix-2 and array multiplier. The simulation result is shown in Fig 3.

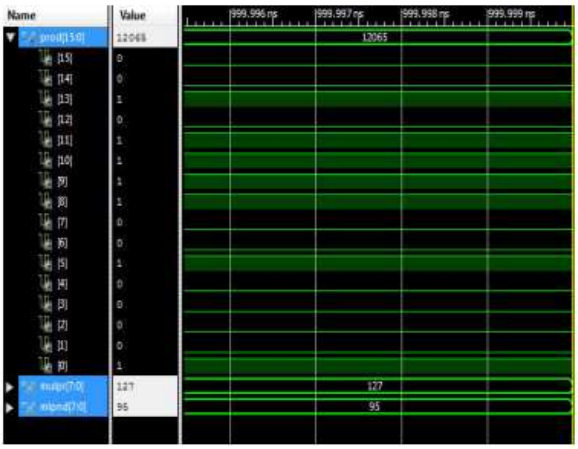

Fig-3: Simulation result of the proposed multiplier design

Figure 4 shows the combinational path delay comparison of the radix-2, array and proposed multiplier.

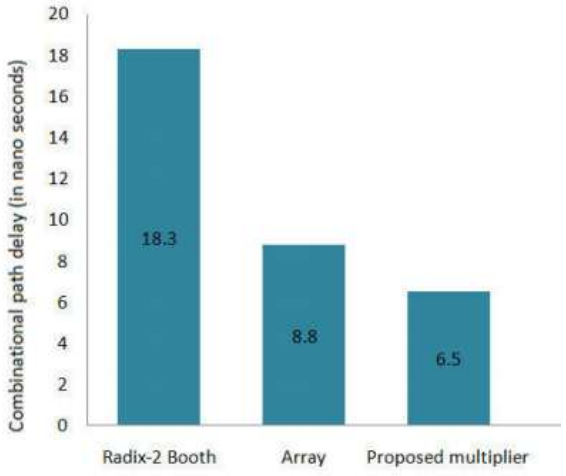

Fig-4: Comparison of the combinational path delay between radix-2, array and proposed multipliers

The speed of the multiplication can be optimized even more by handling partial products produced by the positive triplets resulting from multiplier grouping efficiently.

The on chip power consumption is reduced in proposed design. Since more power consumption occur mainly due to the partial product additions, taking this multiplication phase as a concern, in our design novel adder is designed so that zero carry bits and their addition are handled efficiently by the modified novel carry select adder. Figure 5 shows the onchip power utilization comparison of the radix-2, array and proposed multiplier, onchip power consumption of the proposed multiplier is nearly equal to half of the onchip power consumption of the conventional booth multiplier.

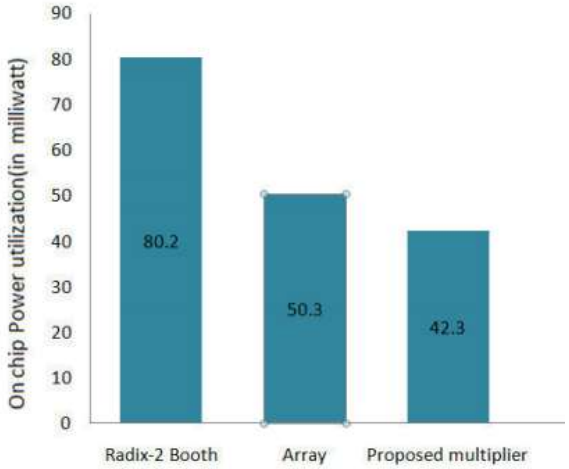

Fig-5: Comparison of the onchip power utilization

Since zero carry bits and additions are handled efficiently by the different adders and respective multiplexers the dynamic power consumption is reduced.

CONCLUSION

Since individual bits of partial products are handled carefully by the carry zero adder/carry non zero adders and respective multiplexers, power consumption due to zero carrys are eliminated successfully in the design. During the implementation it was found that by efficient handling of bus width of positive triplet resulting partial products the combinational path delay was reduced to very good extent.

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